REMARKS

INTRODUCTION

In accordance with the foregoing, claims 1, 3, 15, 21, 23, 33, 35 and 37 have been amended. Claims 2, 17-20, 22, 27, 29-32 and 34 have been cancelled. Claims 1, 3-13, 15, 21, 23, 24, 33 and 35-37 are pending and under consideration.

OBJECTION TO THE CLAIMS

Claim 33 was objected to for reciting an apparatus without any hardware. Appropriate correction consistent with the Examiner's suggestion has been made to claim 33.

Withdrawal of the foregoing objection is requested.

CLAIM REJECTIONS - 35 USC 102

Claims 1-13, 19-24 and 33-37 were rejected under 35 USC §102(e) as being anticipated by Owa et al. (US 6,564,009) (hereinafter, "Owa").

Owa discusses an apparatus for recording and/or reproducing data onto and/or from an optical disk and a method thereof. In Owa, as shown in FIG. 13, the recording and reproducing circuit 53 forms an ECC data block (182 bytes x 208 bytes) by 16 of the sector data blocks. That is, the recording and reproducing circuit 53 may arrange 16 of the sector data blocks each comprising 2048 bytes + 16 bytes by a unit of 172 bytes successively in the order of raster scanning and form error correction code (PI) comprising inner code in the horizontal direction and error correction code (PO) comprising outer code in the vertical direction. Furthermore, the recording and reproducing circuit 53 may interleave the ECC block and form a frame structure shown by FIG. 14. That is, the recording and reproducing circuit 53 may allocate a frame synchronizing signal (FS) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes x 208 bytes thereby forming 412 frames by one ECC data block. The recording and reproducing circuit 53 may form data of 1 cluster having the frame structure shown in FIG. 14 and may allocate the one cluster to 4 continuous sectors. Owa, 18:50-18:67 and Figures 13 and 14.

In Owa, in the optical disk device 110, the wobble data ADIP is detected from the push pull signal PP obtained from the optical head 11 by which the position of irradiating laser beam is detected. A frame address detecting circuit 137 receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal by a built-in band-pass filter. The frame

address detecting circuit 137 decodes the wobble data ADIP by detecting a change in the phase of the wobble signal and executing predetermined signal processing and outputs the decoded wobble data ADIP to a system control circuit 134 and the cluster counter 138. Based upon the received decoded wobble data ADIP, the system control circuit 134 can specify generally the position of irradiating laser beam and the cluster counter 38 can recognize timing of frame synchronization. In the frame address detecting circuit 137, error detection processing may be carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data ADIP which has been determined correct. Owa, 41:6-41:31.

Further in Owa, the optical disk device 170 may include a wobble signal processing circuit 173 which samples the wobble signal WB from the push pull signal PP, processes the wobble signal WB and forms the wobble clock WCK, the clock CK and the reading/writing clock R/W CK. Further, the wobble signal processing circuit 173 detects the wobble data ADIP from the wobble signal WB and supplies the same to the system control circuit 134. Owa, 45:18-45:25 and Figure 51.

Owa discusses that the wobble signal processing circuit 173 amplifies the push pull signal PP by an amplifier circuit 182 having predetermined gain and, thereafter, samples the wobble signal WB by way of a band-pass filter. A comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB. In this way, either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. A phase comparing circuit (PC) 184 which may include an EXCLUSIVE OR circuit compares phases of the wobble clock WCK and the wobble signal WB and outputs a result SCOM of such phase comparison. Owa, 45:26-45:44 and Figures 52A-52G.

Claims 1-13

Amended claim 1 recites: "...performing a logic operation on the window signal generated indicative of the recording allowable range and the encoding block synchronous signal and detecting whether an encoding block boundary is within the allowable range." Support for this amendment may be found in at least original claim 2. In contrast to claim 1, Owa does not discuss a window signal or performing a logic operation indicative of the recording

allowable range and the encoding block synchronous signal and detecting whether an encoding block boundary is within the allowable range. As discussed in the Office Action, in Owa the wobble signal processing circuit 173 amplifies the push pull signal PP and samples the wobble signal WB. A comparing circuit 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB. This detects either a rising edge or a falling edge of the binarized signal S2 rather than the window signal as is recited in amended claim 1. Instead of the window signal, in Owa, one of the rising edge or the falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. As such, no window signal is provided and the logic operation performed by the phase comparing circuit (PC) 184 (including an EXCLUSIVE OR circuit) comparing phases of the wobble clock WCK and the wobble signal WB and outputting a result SCOM does not correspond to the logic operation of claim 1.

Claim 2 has been cancelled. Claims 3-13 depend from claim 1 and are therefore believed to be allowable for the foregoing reasons.

Withdrawal of the foregoing rejection is respectfully requested.

Claims 19 and 20

Claims 19 and 20 have been cancelled.

Claims 21-24

Amended claim 21 recites: "...a first logic gate and a third logic gate performing a logic operation on the first window signal, the third window signal, and the encoding block synchronous signal and detecting therefrom whether the block boundary signal and the encoding block synchronous signal are within a recording allowable range." Support for this amendment may be found in at least original claim 22. Similar to the argument for claim 1, in contrast to claim 21, Owa does not discuss a first or third window signal and the logic operation performed by the phase comparing circuit (PC) 184 of Owa comparing phases of the wobble clock WCK and the wobble signal WB and outputting a result SCOM does not correspond to the logic operation of claim 21.

Claim 22 has been cancelled. Claims 23 and 24 depend from claim 21 and are therefore believed to be allowable for at least the foregoing reasons. Withdrawal of the foregoing

rejections is respectfully requested.

Claims 33-37

Amended claim 33 recites: "...a second window signal generator generating a second window signal detecting whether the block boundary signal and the encoding block synchronous signal exist within a range..." Support for this amendment may be found in at least original claim 34. Similar to the argument for claims 1 and 21, in contrast to claim 33, Owa does not discuss a second window signal generator the logic operation performed by the phase comparing circuit (PC) 184 of Owa comparing phases of the wobble clock WCK and the wobble signal WB and outputting a result SCOM does not correspond to the window signals of claim 33.

Claim 34 has been cancelled. Claims 35-37 depend from claim 33 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejections is respectfully requested.

CLAIM REJECTIONS - 35 USC 103.

Claims 15, 17, 18, 27 and 29-32 were rejected under 35 USC §103(a) as being unpatentable over Owa in view of Ueki (US 6,678,236) (hereinafter "Ueki").

Ueki discusses a method and apparatus for recording information on a recording medium. In Ueki, a first portion of the 1-ECC block data is recorded while the LPP-based recording timing signal is used as reference timings indicative of the boundaries between sectors or the heads of sectors. The timing corresponding to the starting edge of the pre-pit area PR and given by the LPP-based recording timing signal, the system controller 9 suspends the recording and changes the operation of the apparatus from the recording mode to the playback mode. Ueki, 26:45-26:55.

Claims 15, 17 and 18

Amended claim 15 recites: "...recording or stopping recording, according to the states of the first interrupt signal, the second interrupt signal, and the third interrupt signal." Support for this amendment may be found in at least original claims 17 and 18. As previously argued, the Applicant maintains that the combination of Owa and Ueki do not discuss the use of interrupts as is recited in claim 15. In Owa, the timing clock is generated by the operation of the PLL based on wobble signal. The read/write circuit of Owa modulates data in accordance with the

R/W clock and outputs cluster data in accordance with a timing pulse from a cluster counter. As such, the system controller 9 of Ueki suspending the recording would not give better control to the system of Owa since Ueki delays the writing of data to skip a pre-pitted area at the beginning of a sector. In Owa, the recording/reproducing speed is controlled according to bit rate, not block boundary violation.

In claim 2, the window signals are for detecting leading and lagging of the encoding block sync signal with respect to the block boundary. The encoding block sync signal must coincide with the block boundary. Three window signals are respectively generated at the block boundary, prior to the block boundary and after the block boundary. The window signals are generated based on the output of the LPP/ADIP decoder as shown in Figure 2.

Referring to column 46 of Owa, S2, which controls a counting operation of the counter 189, is a binarized signal of a wobble signal WB, and has no relationship with the block boundary on the disk.

In the meantime, as is also known, the wobble signal indicates binary states according to its phase, that is, the wobble signal is a phase modulated pulse signal. For example, if a state where the wobble signal leads by Φ indicates "1," the other state where the wobble signal lags by Φ indicates "0." See Figure 49D of Owa.

According to Owa, the counter 189 performs an up-counting operation when the wobble signal is positive and performs a down-counting operation when the wobble signal is negative. Thus, if the wobble signal leads by Φ, then the count result during a cycle of the wobble signal is high (H1), and if the wobble signal lags by Φ, then the count result is low (L1). The FF 190 shifts the count results by a half cycle of the wobble signal and subtracting circuit 191 determines the difference between the input and the output of the FF 190. Thus, by referring to the output of the subtracting circuit 191, an ADIP signal can be decoded. That is, if the difference is a low value (L2), the corresponding ADIP is in a high state ("1"), and if the difference is a high value (H2), the corresponding ADIP is in a low state ("0"). The middle of the period when the subtracted value is) indicates a falling edge or a rising edge of the ADIP. See Figures 51 and 53 of Owa.

However, the ADIP does not relate to the boundary of blocks on the disk. Also, there is no description in and/or suggestion in Owa to detect whether a signal is in one of a leading,

coinciding and lagging state with respect to a block boundary. Further, the algorithm of the present invention is far different from that of Owa.

Still further, referring to Figure 2 of the present invention, the window signals can be generated based on the ADIP instead of the wobble signal.

Claims 17 and 18 have been cancelled.

Withdrawal of the foregoing rejections is respectfully requested.

Claims 27 and 29-32

Claims 27 and 29-32 have been cancelled.

CONCLUSION

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

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Respectfully submitted,

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